Application Note 383
DS3131 BoSS Initialization Steps

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OVERVIEW

By design, upon power-up the BoSS will not take control of the PCI bus. All the physical ports will send all ones (not the HDLC idle code) and, therefore, the BoSS will be idle upon power-up. On the other hand, the BoSS uses RAM base memory, direct and indirect, to store the states of the internal state machines. Because there are many very complex state machines and interworking functional blocks of BoSS, upon power-up all the internal registers must be initialized to a known state before any data packets can be transmitted and received.

It is recommended that user follow this initialization sequence before sending packetized data.

INITIALIZATION STEP	COMMENTS
1) System reset	System reset can be invoked by either hardware action through the PRST* signal or software action through the RST control bit in the Master Reset and ID register. All configuration registers are set to zero (0000h) by system reset.
2) Configure Local Bus Bridge Mode Control (LBBMC) register	Please note that this register is not affected by the software-invoked system reset. It will be forced to all zeros only by the hardware reset.
3) Configure PCI	This is achieved by asserting the PIDSEL signal.
4) Disable Transmit & Receive DMA for each channel	Make sure the DMA is off on both Transmit and Receive side through the Channel Enable bit in the Transmit and Receive RAM.
5) Configure Receive DMA	Program the Receive DMA Configuration RAM.
6) Configure Receive FIFO	Program the Receive FIFO Registers.
7) Configure Receive Layer 1	Program the Receive Port Registers (RP[n]CR).
8) Configure Transmit DMA	Program the Transmit DMA Configuration RAM.
9) Configure Transmit FIFO	Program the Transmit FIFO Registers.
10) Configure Transmit Layer 2	Program the Transmit HDLC Port Control Registers (TH[n]CR).
11) Configure Transmit Layer 1	Program the Transmit Port Registers (TP[n]CR).
12) Configure Receive Layer 2	Program the Receive HDLC Port Control Registers (RH[n]CR).
13) Enable Receive DMA for each channel	Set the Channel Enable bit in the Receive DMA Configuration RAM for the channels will use.
14) Enable Transmit DMA for each channel	Set the Channel Enable bit in the Transmit DMA Configuration RAM for the channels will use.
15) Configure Interrupts	Optional.
16) Configure Master Control Register	Set the RDE and TDE control bits in the Master Configuration (MC) register.

Note: It is recommended that a “Hardware Reset” be applied to the DS3131 upon power-up.

** Active-low signal.*